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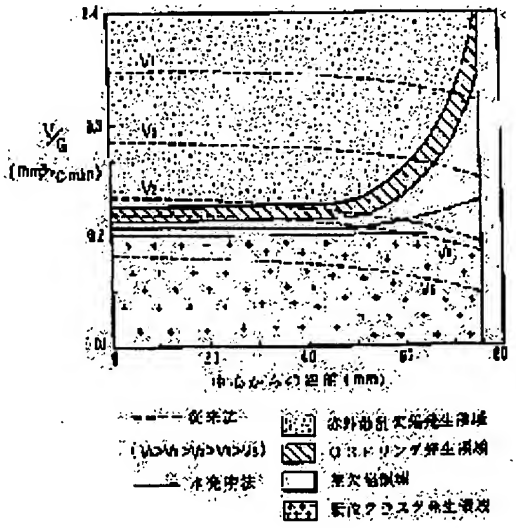
(54) SILICON SINGLE CRYSTAL WAFER AND ITS PRODUCTION

(57)Abstract:

PURPOSE: To provide a silicon single crystal wafer having no grown-in defect over the entire surface.

CONSTITUTION: When a silicon single crystal is grown by Czochralski method at a pulling rate of V (mm/min) with an average temperature gradient of G (°C/mm) in the crystal in the direction of pulling axis over a temperature range from the melting point of silicon and 1300°C, the value of V/G is set at 0.20-0.22 mm2/°C.min between the center of crystal and a position separated by 30 mm from the outer circumference of crystal. The value of V/G is set at 0.20-0.22 mm2/°C.min between the position separated by 30mm from the outer circumference of crystal and the position on the outer circumference of crystal or it is increased gradually toward the outer circumference of crystal. Consequently, the OSF ring disappears in the center of wafer and no dislocation cluster is generated on the outside of the ring.



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* NOTICES *

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2.**** shows the word which can not be translated.
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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the silicon single crystal wafer used for manufacture of a semiconductor device etc. especially the silicon single crystal wafer raised by the Czochrlski method (henceforth a CZ process), and its manufacture approach.
[0002]
[Description of the Prior Art] The silicon single crystal wafer used for manufacture of a semiconductor device is mainly manufactured by the CZ process. A CZ process raises a cylinder-like silicon single crystal by pulling up seed crystal, soaking seed crystal in the silicon melt in quartz crucible, and rotating quartz crucible and seed crystal like common knowledge. the raising rate, i.e., the single-crystal-growth rate, at this time -- usually -- 1.0 - 2.0 mm/min it is .
[0003] By the way, the silicon single crystal wafer raised by such CZ process may produce the oxidation induction stacking fault called OSF generated in the shape of a ring, when thermal oxidation processing (for example, 1000-1200 degree-Cx 1 - 10 hours) is received. This OSF ring is a high-speed raising rate, i.e., 1.0 - 2.0 mm/min, comparatively so that moving to the periphery side of a single crystal may be known as a raising rate becomes quick, and an OSF ring may be distributed over manufacture current [LSI] at the outermost periphery of a single crystal. The raised high-speed training wafer is used.
[0004] However, several sorts of minute defects (a Grown-in defect is called below) exist in the silicon single crystal wafer raised at such a high speed, and it is becoming clear to degrade the gate oxide proof-pressure property of an MOS device. Moreover, since these Grown-in defects are very stable thermally, they are not extinguished in the manufacture process of a device, but remain to the active region near the wafer front face, and it is becoming clear not only an oxide-film proof-pressure property but to degrade a junction leak property (for example, M.Horikawa et al.Semiconductor Silicon 1994, p987).
[0005] Since gate oxide was thin-film-ized in recent years with degree-of-integration increase of MOS mold quantity integrated semiconductor components, such as LSI, and the diffusion layer depth, such as a source drain, became shallow, the improvement in the withstand voltage property of gate oxide and reduction of junction leakage current are demanded strongly, but since these properties are inferior in the high-speed training wafer currently used for manufacture current [LSI], to the latest high degree of integration, correspondence is becoming difficult especially.
[0006] Then, raising rates are recently 0.8 mm/min. The method of raising a silicon single crystal at the following medium speed or low speeds was proposed by JP,2-267195,A. However, there is a trouble on the following crystal quality also in the silicon single crystal wafer raised at such a medium speed - a low speed.
[0007]
[Problem(s) to be Solved by the Invention] Generally, even if it depends for the temperature distribution in a single crystal on the structure in CZ furnace and a raising rate changes, the distribution does not change a lot. Therefore, if a raising rate is changed and a single crystal is raised with the equipment which has the same structure, the relation of a raising rate and defective generating distribution as shown

in drawing 1 will be seen. Although this relation will change a little if equipment differs, it does not change to an inclination.
[0008] A raising rate is 0.8 - 0.6 mm/min. In being medium-speed training, as shown in this drawing (A), it generates an OSF ring near [1/2] the radius of a silicon single crystal wafer. Physical properties differ by the outside and the inside of a ring, and the proof-pressure property of gate oxide is good in the field outside an OSF ring.
[0009] However, in the field inside a ring, since some kinds of Grown-in defects exist, the proof-pressure property is not good. The infrared dispersion defect which is formed during crystal training and observed by the infrared tomograph method in the state of as-grown especially is about 106. An individual / cm3 It generates by the consistency. Since this defect considered to be an oxygen sludge is very stable thermally, it does not disappear in the heat treatment process of a device, either, it remains to a device active region, and a junction leak property is also degraded.
[0010] Moreover, it generates by width of face of several mm - about 10mm, and the OSF ring itself is about 104. An individual / cm2 Since OSF is included by high density, it becomes the cause of worsening, the property, for example, junction leak property, of a semiconductor device. Furthermore, in this field, when a wafer is heat-treated, an oxygen sludge is generated by the consistency of 108 -109 cm-3. The nucleus of this oxygen sludge is also thermally stable, and even 1250-degree C heat treatment grows. Therefore, it becomes the cause by which the OSF ring itself degrades the property after a device process.
[0011] It is the raising rate of a silicon single crystal 0.6 - 0.5 mm/min When it is made to fall, as shown in drawing 1 (B), the diameter of an OSF ring becomes still smaller and OSF occurs near the core of a wafer at the shape of a ring, and discoid. Although an oxide-film proof-pressure property improves since the area outside a ring increases, instead, a rearrangement cluster occurs in the periphery section of a ring outside. For magnitude, a consistency is [this rearrangement cluster] about 103 at about 10-20 micrometers. An individual / cm2 It is extent and it is well known to become the cause by which this also degrades the property of a semiconductor device.
[0012] Moreover, in the silicon single crystal wafer raised by the CZ process, an oxygen impurity is 1 - 2x1018 atoms/cm3. It is contained by concentration. And it is as having mentioned above that precipitation of oxygen happens by heat treatment (for example, dozens of 600-1150 degree-Cx hours) in a device process for this oxygen impurity. While this oxygen sludge is generated in a device active region and degrades the property of a device, it acts as a site which carries out gettering of the heavy metal contamination generated in a device process.
[0013] In the field inside an OSF ring, since precipitation of oxygen happens strongly, the usual in thorin chic gettering ability (henceforth IG ability) is obtained, but in the field which the rearrangement cluster outside an OSF ring generates, since this precipitation of oxygen cannot happen easily, IG ability falls.
[0014] Thus, a raising rate is 0.8 - 0.5 mm/min. Since an OSF ring remains, there is nothing as the ring itself is a defective generating field, and a defect occurs also within and without a ring, the wafer raised with medium speed does not fit manufacture of the semiconductor device of a high degree of integration.
[0015] On the other hand, raising rates are 0.5 mm/min. With the wafer raised at the following low speeds, as shown in drawing 1 (C), an OSF ring field disappears in the center section of the wafer, and the field which the infrared dispersion defect inside a ring generates in connection with this also disappears. However, a rearrangement cluster occurs all over a wafer. It is as having mentioned above that generating of a rearrangement cluster causes a fall of a device property and a fall of IG ability. Therefore, a low-speed training wafer does not fit manufacture of a highly-integrated semiconductor device, either.
[0016] As mentioned above, in training of the silicon single crystal by the present CZ process, however it may adjust a raising rate, a harmful defect will arise in a part of direction [at least] of the diameter of a crystal, and the wafer of a whole surface non-defect will not be manufactured.
[0017] The purpose of this invention is in the thing which do not have a harmful defect over the whole

surface and for which the silicon single crystal wafer and its manufacture approach of quality CZ process training are offered.

[0018]

[Means for Solving the Problem] By the way, this invention persons acquired the important following facts about the generating location of an OSF ring previously.

[0019] Although the path of an OSF ring changes depending on the raising rate of a crystal and the path decreases with the fall of a raising rate with the crystal training equipment which has the same structure, when training equipment is different and hot zone structure changes, even if it is the same raising rate, the paths of an OSF ring differ. However, when setting the raising rate of a single crystal to V (mm/min) and setting the average of inclination to G (degree C/mm) whenever [crystal internal temperature / of the raising shaft orientations in the pyrosphere from the silicon melting point to 1300 degrees C], the path of an OSF ring is uniquely determined by the ratio expressed with V/G. That is, it becomes possible by controlling V/G value to be able to generate the location with an eye on an OSF ring, and to also make it disappear.

[0020] However, even if it controls the generating location of an OSF ring by control of V/G value, it cannot be made to disappear to Grown-in defects, such as an infrared dispersion defect and a rearrangement cluster.

[0021] Then, this invention persons investigated as follows the effect of V/G value exerted on defective distribution. Temperature distribution in case a solid-liquid interface is in each location of 100,200,300,400mm from the shoulder of a single crystal, respectively were searched for in comprehensive heat transfer analysis. if the effectiveness of the temperature distribution by the convection current in melt is not taken into consideration in this heat transfer analysis -- actually -- ** -- we are anxious about a different solid-liquid interface configuration being acquired, and the temperature distribution in the elevated-temperature section near especially a solid-liquid interface in a crystal changing an actual thing and a little with these. The problem on this count has been solved, in order to acquire exact temperature distribution rather than it can set in the elevated-temperature section, the configuration of the solid-liquid interface in each above-mentioned location was further measured from the real crystal, the shaft-orientations temperature distribution inside a crystal were again calculated as the melting point of silicon by having made temperature on the front face of a crystal according the temperature in an interface to this and the above-mentioned thermal rating into boundary condition, and the direction distribution of a path of a shaft-orientations temperature gradient was calculated after this. The axis of abscissa was set as the direction location of a path, and drawing 2 showed defective distribution by setting an axis of ordinate as V/G value.

[0022] V/G value is 0.20mm2 / **, and min so that drawing 2 may show. When it is the following, a rearrangement cluster occurs in the direction whole region of a path. V/G value is 0.20mm2 / **, and min. It takes for becoming large and a field changes in order of a defect-free field and OSF ring generating field and an infrared dispersion defective generating field. Although the minimum of a defect-free field is regularity (0.20mm2 / **, and min) regardless of the direction location of a path here, between a crystal center and the location from a crystal periphery to 30mm, an upper limit is fixed (0.22mm2 / **, and min), between the location from a crystal periphery to 30mm, and a crystal periphery location, is taken for approaching a crystal periphery and serves as size. And even when hot zone structures differ, various defects are distributed according to this drawing.

[0023] That is, if it pulls up with hot zone structure and a rate is decided, V/G value in the direction of the diameter of a crystal which the training equipment has will be determined like a broken line. a raising rate -- V1 it is -- a case -- the V/G curve -- an infrared dispersion defective generating field -- crossing -- a crystal -- a part -- an infrared dispersion defect -- being generated -- an OSF ring generating field -- crossing -- a crystal -- a part -- an OSF ring -- generating . Therefore, it pulls up and a rate is V1. An OSF ring is generated in the outermost periphery of a wafer, and an infrared dispersion defect produces a case in the field of the inside. When a raising rate falls, a V/G curve is V2, V3, V4, and V5. It moves like and the direction distribution of a path of the defect generated into a crystal changes.

[0024] In that V/G which becomes defect-free in the direction whole region of a path of a single crystal

in training of the silicon single crystal by the CZ process exists, that it is possible to abolish a defect in the direction whole region of a path of a single crystal depending on V/G if it puts in another way, however the conventional training, since the lower right generally serves as [a V/G curve] ** regardless of the raising rate of a single crystal, it is two points of being unable to perform supposing that it is defect-free in the direction whole region of a path points should be observed here.

[0025] Although a V/G curve describes in detail that the lower right serves as ** later, the shaft-orientations temperature gradient in a crystal is because it is large in the periphery section as compared with a core. Namely, since G takes toward a periphery from a core and V increases in the fixed condition, as for a V/G curve, the lower right serves as **. Therefore, although V/G which becomes defect-free in the whole region of the direction of a path exists, the whole wafer surface cannot be made defect-free.

[0026] For example, VV1 An OSF ring is generated in the outermost periphery of a wafer, and an infrared dispersion defect generates a case in the inside. This is high-speed training of the general former. VV1 V2 [late] and V3 Although an OSF ring will be generated in the direction pars intermedia of a path of a wafer and the outside will serve as a defect-free field if it becomes, inside, an infrared dispersion defect occurs. This is medium-speed training and is equivalent to drawing 1 (A). V is V4 [still later]. Although an OSF ring will be generated in a wafer core and a defect-free field will remain in the outside if it becomes, a rearrangement cluster occurs in the outermost periphery. This is medium-speed training equivalent to drawing 1 (B). V is V5 [still later]. Although an OSF ring will disappear in a core if it becomes, a rearrangement cluster occurs all over a wafer. This is low-speed training equivalent to drawing 1 (C). Moreover, 0.20-0.22mm2 / **, and min from which a defect does not produce V/G in the crystal center section temporarily Even if it manages, in order to take for separating from the crystal center section and for V/G to fall, a rearrangement cluster is produced except a core.

[0027] Thus, in training of the silicon single crystal by the CZ process, although V/G which can form a defect-free field in the direction whole region of a path of a single crystal exists, since the lower right is the curve of **, V/G cannot make the whole wafer surface defect-free.

[0028] However, if V/G can be made into a straight line fixed in the direction of a path, or the curve of right going up increased gradually in the periphery section in the direction of a path of a single crystal, generating of a defect can be prevented in the whole region of the direction of a path. Based on this assumption, this invention persons performed further investigation analysis. Consequently, it can consider as a straight line as shows V/G to drawing 2 as a continuous line depending on the structure of the hot zone of crystal training equipment, or the curve after the right, consequently a defect-free field is formed in the direction whole region of a path of a single crystal, the knowledge of manufacture of the whole surface defect-free wafer which was impossible until now being attained here is carried out, and it came to complete this invention.

[0029] The silicon single crystal wafer of this invention is a silicon single crystal wafer raised by the CZ process, when it carries out thermal oxidation processing, it is a low-speed training wafer with which the oxidation induction stacking fault (OSF) generated in the shape of a ring was extinguished in the wafer core, and it is characterized by eliminating the rearrangement cluster from the whole wafer surface.

[0030] Moreover, in case the wafer manufacture approach of this invention raises a silicon single crystal by the CZ process When setting a raising rate to V (mm/min) and setting the average of inclination to G (degree C/min) whenever [crystal internal temperature / of the raising shaft orientations in the temperature requirement from the silicon melting point to 1300 degrees C], Between a crystal center location and the location from a crystal periphery to 30mm, they are 0.20-0.22mm2 / **, and min about V/G value. It carries out. Between the location from a crystal periphery to 30mm, and a crystal periphery location, they are 0.20-0.22mm2 / **, and min. It is characterized by carrying out or making it increase gradually toward a crystal periphery.

[0031]

[Function] Since an OSF ring is the low-speed training wafer which disappeared in the wafer core, the wafer of this invention does not include the infrared dispersion defect generated in OSF and its inside. And the rearrangement cluster which should be generated outside is also eliminated. Therefore, it

becomes the high quality wafer which does not have a harmful defect over the whole surface.
[0032] Moreover, by the wafer manufacture approach of this invention, the temperature distribution of CZ furnace are adjusted so that V/G value may cross only a defect-free field in the direction of the diameter of a crystal. The lower limit of a defect-free field is 0.20mm2 / **, and min here. A upper limit is set into the part it is fixed and excluding 30mm from a periphery, and they are 0.22mm2 / **, and min. It is fixed and the gradual increase is carried out toward the periphery in the part from a periphery to 30mm. Therefore, between a crystal center location and the location from a crystal periphery to 30mm, they are 0.20-0.22mm2 / **, and min about V/G value. It carries out. Between the location from a crystal periphery to 30mm, and a crystal periphery location, they are 0.20-0.22mm2 / **, and min. By carrying out or making it increase gradually toward a crystal periphery, the low-speed training crystal which an OSF ring disappears in the crystal center section, and does not contain a rearrangement cluster is obtained.
[0033] Generally the shaft-orientations temperature gradient in a crystal has the large periphery section as compared with a core. It is this having the exoergic section in CZ furnace below a crystal, and the heat flow rate which flowed from the solid-liquid interface since the upper part of a crystal and a perimeter were the low-temperature sections pulling up under a crystal, meeting a shaft, and flowing toward the upper part and the direction of a front face of a crystal (periphery). It is because a crystal is cooled, and the heat dissipation from a crystal front face is as large as the furnace at which a crystal is easy to be cooled, and the temperature gradient in the periphery section tends to become large. Therefore, at general CZ furnace which has the structure where crystal cooling power is large, the direction distribution of a path of V/G in the crystal under growth has the inclination to fall toward a periphery from a core, at a fixed raising rate. At such a CZ furnace, even if V/G value is in the defect-free field of drawing 2 in a core, if a periphery is approached, it will separate from this field, and in order to cross the field which a rearrangement cluster generates, generating of a rearrangement cluster is not avoided.
[0034] However, since, as for CZ furnace at which a crystal is hard to be cooled, the direction of a heat flow rate mainly flows toward the upper part conversely rather than a periphery and, as for the crystal front face of the elevated-temperature section conversely near the melting point, temperature tends to become high relatively by radiation from melt, quartz crucible, a heater, etc., a temperature gradient becomes low a little rather than a core. However, in the heat dissipation from a crystal front face, for a certain reason, a temperature gradient does not become small without any restriction not a little. At CZ furnace which has the structure where a crystal is hard to be cooled, V/G value serves as an inclination which increases 1 certain or a little in the direction of a path, and does not increase without any restriction from this. Therefore, if such a CZ furnace is used and V/G value is made to exist in a defect-free field in the crystal center section, in the direction whole region of a path, it will not separate from V/G value from a defect-free field. Consequently, though an OSF ring is the low-speed training crystal which disappeared in the core of a crystal, the single crystal which a rearrangement cluster does not generate is obtained.
[0035] The temperature gradient in the elevated-temperature section near the melting point in a crystal is not necessarily fixed in a crystal orientation, and it changes from the top section a little, applying it to a tail part. This is for the heat flow rate which carries out an inflow outflow to change to a crystal, when the thermal environment in CZ furnace changes with change of that heater power changes in order to maintain a fixed diameter at the time of crystal growth, crystal length, residual melt volume, etc., etc. gradually. Therefore, in the conventional CZ process, the defective distribution which V/G value also changes and generates it also changes with change of the temperature gradient of the crystal orientation accompanying increase of the amount of raising to shaft orientations every only (refer to drawing 3).
[0036] Then, to change of the temperature gradient G of a crystal orientation, it pulls up so that V/G may become fixed, and a rate V is adjusted (refer to drawing 5). doing so -- the shaft-orientations whole region -- also setting -- the whole surface -- it becomes possible to suppose that it is defect-free. Thus, even if it pulls up for the purpose of defective control and controls a rate, diameter control of a crystal is possible as usual. That is, though it pulls up by the fixed span for every time amount for several seconds

and a rate is fluctuated control and it of heater power, linkage, or around a target raising rate independently required for defective control, the average raising rate V does not change but V/G value made into the purpose are maintained. This is because generating of a defect is not influenced to fluctuation of the raising rate of such a short time.

[0037]

[Example] The example of this invention is explained below.

[0038] In CZ furnace which can raise 18"6 in which quartz crucible and carbon crucible were installed" single crystal The relative position of the cylinder-like carbon heater and crucible which were installed in the perimeter of crucible, The distance of the tip of the radiation screen of 5mm in thickness, and the semicircle drill configuration of 200mm of diameters of opening and melt front face which consist of carbon installed in the perimeter of a training crystal, The comprehensive thermal rating examined conditions variously, in parts except the field from a crystal periphery to 30mm, such as heat insulator structure of the perimeter of a heater, V/G was almost fixed, and the above-mentioned conditions were determined so that V/G might increase in monotone toward a periphery in the field from a periphery to 30mm. A count result is shown in drawing 3 . 0,100--700mm in drawing is the amount of crystal raising.

[0039] After determining the above-mentioned conditions, 65kg of high grade polycrystalline silicon is put into 18" quartz crucible, boron is doped, the heating dissolution of the polycrystalline silicon is carried out, crystal growth bearing pulls up [a diameter] the single crystal of <100> by 150mm, and rates are 0.45 mm/min. It raised to die length of 1300mm at a low speed.

[0040] the crystal after training -- a crystal orientation and parallel -- 1.5mm in thickness -- starting -- HF and HNO3 from -- dissolution removal of the processing distortion is carried out in the becoming mixed-acid solution, and it is further immersed into a rare HF solution, and the rinse was carried out and it was made to dry with ultrapure water after that After heat-treating this sample in 800 degrees C / 4hr+1000 degrees C /, and 16hr desiccation oxygen, the X-ray topograph investigated generating distribution of a defect. Although distribution of a defect was shown in drawing 4 , distribution of the investigated defect became a thing corresponding to the count result of drawing 3 as follows. In addition, the figure in drawing 4 is the die length from the shoulder of a single crystal, and corresponds to the amount of raising in drawing 3 .

[0041] a ratio with the average G of the crystal orientation temperature gradient from the raising rate V and the melting point to 1300 degrees C -- in the direction of a path of a crystal, V/G is about 1 constant value from a core up to the location of 45mm, and is increasing in monotone toward the periphery section from the location of 45mm. In addition, the location of 45mm is 30mm in location from a periphery from a core.

[0042] As a result of managing V/G in this way, in the shaft-orientations part from the crystal top to 200mm, V/G in the crystal center section is 0.20mm2 / **, and min. It is the following and the rearrangement cluster occurred throughout the direction of a path. If it applies to 500mm from 200mm, V/G in the crystal center section is 0.22-0.20mm2 / **, and min. It has become. At about 400mm, V/G is especially 0.22-0.20mm2 / **, and min in the field from a crystal center to 45mm. It is maintained. Since V/G increased from 45mm in monotone in the outside field and V/G was managed by these in the defect-free field throughout the direction of a path, generating of the harmful Grown-in defect of others, such as an OSF ring and an infrared dispersion defect, was not seen throughout the direction of a path. In the part applied to a crystal tail from 500mm, V/G in the crystal center section is 0.22mm2 / **, and min. Since it exceeded, the OSF ring was generated and the infrared dispersion defect occurred in the inside.

[0043] As shown in drawing 5 based on such a result next, the about 400mm [in said example] V/G curve was reproduced in the overall length of a crystal orientation. That is, V/G is 0.22-0.20mm2 / **, and min in the field from a crystal center to 45mm. It was maintained, and the target raising rate in a crystal orientation was set up so that V/G might increase from 45mm in monotone in an outside field. Other operating conditions except a raising rate were set up like said example, and raised the single crystal of 6"B dope <100> and 1300mm of crystal length. Generating distribution of the defect in this

crystal was investigated by the same approach as said example. In the overall length applied to a tail part, generating of an OSF ring, an infrared dispersion defect, and a rearrangement cluster was not seen from the top section.

[0044]

[Effect of the Invention] The silicon single crystal wafer of this invention is very stable thermally, remains or grows up to be a device active region, since the harmful Grown-in defect (an infrared dispersion defect, an OSF ring, rearrangement cluster) which degrades the dependability and the junction league property of gate oxide is not include over the whole surface, it is use for a high integrated semiconductor component, prevents the property degradation, and contributes it to improvement in a component manufacture yield, as explain above. Moreover, manufacture of CZ silicon single crystal wafer of such high quality is easily attained by the wafer manufacture approach of this invention.

[Translation done.]